Notice of Allowability	Application No.	Applicant(s)	
	10/000,153	TANAHASHI, TOSHIO	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to *6/17/2005*.

2. ☒ The allowed claim(s) is/are *1-24*.

3. ☒ The drawings filed on *04 December 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Acknowledgment

1. This Office Action is responsive to the Amendment filed on 06/17/2005.

2. Examiner finds Applicants amendment to claims 3 and 17, rejected under 35 U.S.C. 112, second paragraph, office action dated 3/14/2005, acceptable.

3. The Abstract of the Disclosure amended 06/17/2005, is acceptable.

Reasons for Allowance

4. Claims 1-24, allowed.

5. The following is an examiner's statement of reasons for allowance:

With reference to claim 1 and 3, the prior art made of record does not teach or explicitly show, a high-speed transmission system having a low latency and comprising a plurality of first transmitter circuits in a send side and a plurality of first data processing circuits in a receive side respectively, said first transmitter circuit and said first data processing circuits connected one-to-one via a transmission line, said high-speed transmission system comprising:

a plurality of first transmitter circuits each comprising an n(a multiple of 2)-bit register that receives input data with a system clock (CLKSYS) with which input data is prepared by splitting an input parallel data and receives a clock having a-same frequency as that of the above system clock (CLKSYS); and parallel-serial conversion circuits that convert a parallel data signal that is output from said n(a multiple of 2)-bit registers into a serial data signal using a clock for

transmission having a n/2 multiple frequency which was synchronized with the system clock (CLKSYS) or a divided clock of said clock for transmission such that,

when an invalid data string, a regulation signal string that changes surely into 1 and 0, and a first specific signal string comes out at a free or a certain period from said first transmitter circuit so that start times of the invalid data string and a second specific signal string become same and the finish times of the first specific signal string and a third specific signal string become same, a regulation controlling logic circuit generates the second specific signal string, the regulation signal string that changes surely into 1 and 0, and the third specific signal string;

a second transmitter circuit comprising:

a n-bit register that receives an output signal of said regulation controlling logic circuit with the system clock (CLKSYS) or a clock having the a same frequency as that of the system clock (CLKSYS); and

parallel-serial conversion circuits that convert a parallel data signal that is output of said n-bit register into a serial data signal using for transmission a clock for transmission having a n/2 multiple frequency synchronized with the system clock (CLKSYS), or a de-multiplied clock of said clock said plurality of first data processing circuits each comprising:

a DLL circuit that makes phase comparison between an output of the DLL circuit that sets an input the clock for transmission having a an n/2 multiple frequency of the system clock (CLKSYS) synchronized to the clock for transmission used in said first transmitter circuits and a serial data signal from one of said first transmitter circuits to regulate a sampling clock so as to have a timing at a center of data;

sampler and serial-parallel conversion circuits that sample a serial data signal from the sampling clock to convert it into a parallel data signal;

a first start-aligned detection circuit that resets a regulation control signal (strt) indicating a regulation start and a regulation finish of said DLL circuit when the regulation start signal comes out, releases a hold of a flip-flop that stored a lead bit position compares the first specific signal string with a parallel data signal that are outputs from said serial parallel conversion circuits that sets the regulation control signal (strt) in the an event that they accorded when the regulation control signal (strt) was reset, and stores and holds the g-lead bit position;

an alignment circuit that invalidates an output with a regulation control signal (strt) reset by this first start-aligned detection circuit and, according to a storage result of the lead bit position of said first start-aligned detection circuit when the regulation control signal (strt) was set in said first start-aligned detection circuit, outputs n bits starting with a bit next to the signal string that accorded as data every n bits;

a write address generation circuit that stops when the regulation control signal (strt) of said first start-aligned detection circuit is a reset, and generates write addresses that circulate starting with the an address 0 until an (m-1)th addresss when it is a set;

an m-address n-bit FIFO circuit that sequentially mites the an output of said alignment circuit into a designated address according to the an output of this the write address generation circuit;

an m-way n-bit multiplexer that selects a data signal of the address designated by the read address written in said m-address n-bit FIFO circuit being synchronized with the system clock (CLKSYS); and

an n-bit register that writes the an output of this m-way n-bit multiplexer a second data processing circuit comprising:

a DLL circuit that makes a phase comparison between an output of the DLL circuit that sets at the an input the clock for transmission having a an n/2 multiple frequency of the system clock (CLKSYS) synchronized with the clock for transmission used in said second transmitter circuits and a serial data signal from said second transmitter circuits to regulate a sampling clock so as to have a sampling timing at the center of data;

sampler and serial-parallel conversion circuits that sample a serial data signal with a sampling clock to convert it into a parallel data signal;

a second start-aligned detection circuit that compares the an output of said sampler and serial-parallel conversion circuits with the second specific signal string prepares a regulation start signal with a given pulse width indicating regulation of said DLL circuit when they accorded, distributes it to said first data processing circuit resets a regulation finish signal, compares the output of said serial-parallel conversion circuits with a third specific signal string, and sets a regulation finish signal when they accorded;

a synchronizing circuit that synchronizes the regulation finish signal with the system clock (CLKSYS) and outputs a read address start signal at such timing that the read address start signal is output after the output of said alignment circuit was written into said m-address n-bit FIFO circuit and yet before a next data is written into the same address in said m-address n-bit FIFO circuit of said plurality of said first data processing circuits; and

a read address generation circuit that stops when the read address start signal from this synchronizing circuit is reset and distributes the read addresses that is sequentially generated in circulation of an address 0 to an address (m-1) and yet simultaneously designates a same address for a plurality of said m-address n-bit FIFO circuits of said first data processing circuit when a read address start signal from this synchronizing circuit is set.

Such limitations, as recited in claims 1 and 3, are neither anticipated nor rendered obvious by the prior art made of record.

5. Claims 2, and 4-24 are allowed based on dependency to claims highlighted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
July 6, 2005.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER